Evaluation Plan
for
Grid-Tied Photovoltaic Inverters

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1 Introduction

The test plan described below is intended to be a thorough evaluation that can be used for the characterization of any single phase or three-phase grid-tied photovoltaic inverter. Many of the test criteria are from IEEE Standard 929-2000[1]. The anti-islanding tests of section 3.xxx were developed at Sandia's Distributed Energy Technologies Laboratory (DETL) specifically to support that standard. Although IEEE 929 is a recommended interconnection standard for photovoltaic inverters with power outputs below 10 kilowatts, the same set of tests are performed on larger inverters at DETL. These tests also provide useful performance information for power-generating systems using prime power-conversion methods other than PV, such as fuel cells, microturbines, or energy storage systems. The purposes of these characterizations are to:

1. Develop a standard method for evaluating inverters
2. Benchmark inverter capability using a single test methodology,
3. Ensure that users have all necessary information required for system design, and
4. Identify areas where future development may enhance inverter capabilities and performance.

The manufacturer and Sandia may elect to omit some of these tests, depending on the status of the unit under test. Units may be withdrawn for further engineering development based on the result of a specific test so that the entire battery of tests is not completed for that particular development unit. For example, the manufacturer may choose to omit pulse testing due to the possibility of damage.

2 Test Configuration

2.1 DC Power

Although dc power supplies are available, the majority of tests are performed using actual PV power. DETL contains two crystalline-silicon PV arrays that total just over 50 kW_{dc}. The modules of the arrays are configured to provide the operating range required by the inverter under test.

2.2 AC Power

There are a number of points where the inverter under test may be connected to the DETL utility grid. The interconnection location, i.e., "point of common coupling," is selected based on the output voltage and power rating of the inverter. Details of the circuit configuration used will be provided with the test documentation.

2.3 Instrumentation

For all low-frequency measurements (<450 kHz), the following sensors will be used. Radio frequency interference (RFI) is measured using a Farnell spectrum analyzer system designed for that purpose. RFI transducers are Electro-metric Line Impedance Stabilization Networks for conducted RFI and a Farnell RF antenna for radiated RFI.

[1] IEEE 929-2000, Recommended Practice for Utility Interface of Photovoltaic (PV) Systems

Parameter	Location	Sensor	Transfer Function (nominal)
Vdc	Inverter input terminals	Tektronix P5200 differential voltage probe	500 V/V
Idc	DC line input to inverter	Empro 50 mV shunt OSI shunt amplifier	Shunt: sized for inverter OSI: 100V/V
Vac each ϕ	Inverter output terminals	Tektronix P5200 differential voltage probe	500 V/V
Iac each ϕ	Instrumentation	Ion Physics CM-1-L current monitor	10 A/V
Temperature	Inverter heat sink	Type T thermocouple & Omega amplifier	5V = 100°C

Table 1. Instrumentation Matrix

2.4 DAS

The primary data-acquisition system used for these tests is a 16-bit, 330 ksamples/second digitizer controlled by a National Instruments LabVIEW™ program. The system is calibrated end-to-end using NIST-traceable secondary standards. Data is acquired in both averaging and high-speed waveform-acquisition modes.

1. Average data: Voltages and currents are acquired, averaged, and used to calculate basic electrical quantities including rms voltage, rms current, volt-amperes (kVA), power (W), reactive power (var), and power factor.
2. High-speed data: Voltages and currents are processed by LabVIEW virtual instruments to calculate parameters including harmonic distortion, times required to disconnect following voltage perturbations, and times required to disconnect from an island.

Additional instruments are used for indication and independent corroboration. These include Yokogawa Power Meters, Voltech Power Meters, Hewlett-Packard spectrum analyzers, audio analyzers, and precision digital multi-meters, and Fluke harmonic analyzers and multi-meters.

3 Test Plan

Virtually all modern grid-tied PV inverters use some algorithm to extract the maximum power available from the PV array. Without disabling this feature it is generally not straightforward either to request specific power levels from the inverter or to operate it at specific voltage levels. The approach taken at DETL is to evaluate a number of parameters by operating the inverter with a PV array configured to provide maximum rated inverter power. It is recognized that different results may be obtained using arrays with different maximum-power-point voltages and currents, but these differences are generally not significant. It is felt that this method maximizes the amount of useful data that can be obtained in a reasonable testing period.

3.1 Power and Efficiency

3.1.1 Rated power

The PV array is configured so that maximum rated power can be provided to the inverter during mid-day periods of highest irradiance. If the inverter's power rating exceeds the available PV, alternate methods of achieving maximum power will be explored. These include operating from DETL storage batteries or power supplies. These methods generally require disabling of the maximum-power-point tracking.

The manufacturer will be consulted as to whether the inverter is designed to limit its output to protect itself when more dc power is available than the inverter is designed to convert. This protection feature normally consists of operating off the maximum-power point of the array to avoid damaging the power electronics of the inverter. This feature will be tested by oversizing the PV array. If the inverter does not have this internal self-limiting feature, care will be taken not to exceed its dc power rating.

3.1.2 Efficiency

Ac and dc power will be measured over the power range of the inverter. The resulting data will be sorted and efficiency (Pac/Pdc) will be plotted and tabulated as a function of ac power.

3.1.3 Maximum power point tracking

While operating during the course of a sunny day, dc input to the inverter will be interrupted and array I-V curves will be acquired. The inverter will then be reconnected to the array and normal operation resumed. The time required to interrupt operation to take an I-V curve will be limited to not more than one minute. The dc power into the inverter will be compared to the maximum power recorded by the I-V curve tracer. This test will be repeated for five different IV curves (i.e. five different inverter output levels).

3.2 Utility Compatibility

3.2.1 Power factor

Power factor, defined as $P_{ac}/(V_{rms}*I_{rms})$, will be calculated from data acquired throughout the power range of the inverter. This definition includes effects of both distortion and displacement (cos θ). The resulting data will be sorted and power factor will be plotted and tabulated as a function of ac power.

Most grid-tied inverters are designed to operate at unity power factor. If power-factor correction or reactive power (var) dispatch features are part of the design, they will be evaluated.

3.2.2 Harmonic distortion

Total harmonic distortion (THD) is the ratio of the rms value of the sum of the squared individual harmonic amplitudes to the rms value of the fundamental frequency of a complex waveform.

(1) $$THD = (I_2^2 + I_3^2 + I_4^2 + ...)^{1/2} / I_1$$

IEEE 519 (ref 2) specifies allowable total demand distortion (TDD) for nonlinear loads in terms of a percentage of the ***maximum*** demand load current.

(1) $$TDD = (I_2^2 + I_3^2 + I_4^2 + ...)^{1/2} / I_{\max}$$

Voltage and current THD and individual harmonic amplitudes will be measured up to 3 kHz (50th harmonic).[2] Measurements will be made when the inverter is delivering 100% of rated power. Test will only be performed if line voltage harmonics are less than 1% when the inverter is not energized.

3.2.3 DC injection

This test is only of interest for inverters that do not require transformers between their ac outputs and the grid. Both polarities of the inverter output signal will be recorded and integrated so that any dc component can be detected and quantified.

[2] IEEE 519-1992, Standard Practices and Requirements for Harmonic Control in Electrical Power Systems

3.2.4 AC line voltage and frequency variations

Tests described in the following three sections are performed using a controllable ac power supply in place of the grid. DETL uses two such supplies that are manufactured by Elgar and Pacific Power Source. A resistive load is placed on the output of the ac power supply to absorb power from the inverter under test.

3.2.4.1 Steady-state voltage and frequency

Voltage will be varied from nominal in 1.0-V increments until the inverter trips off due to over voltage or under voltage. Frequency will be varied from nominal in 0.1-Hz increments until the inverter trips off due to over frequency or under frequency. Each voltage or frequency value will be maintained for at least ten seconds before proceeding to the next level. The last value at which the inverter operated and the value at which it ceased to operate will be recorded.

3.2.4.2 Voltage disturbances

The conditions of concern are reproduced from paragraph 5.1.1 of IEEE 929. Local loads are not specified for this test. Inverter output power will be less than half of rated power.

Voltage (% of nominal)	**Maximum Trip Time**
(V < 50%)	6 cycles
(50% < V <88%)	120 cycles
(88% ≤ V ≤ 110%)	Normal Operation
(110% < V < 137%)*	120 cycles
(137% < V)*	2 cycles

Table 2. Voltage Disturbances

*Note: IEEE 929 specifies a maximum of 137% of nominal, but the surge voltage will be limited to 600V line-to-line for these tests to avoid overstressing components and insulation. IEEE P1547.1 will address this voltage limitation for distributed generation source testing.

The inverter should provide no energy to the utility after experiencing the following four conditions. Inverter restart time will be monitored and recorded; the restart time allowed by IEEE 929 is not sooner than 5 minutes.

Test 1. A deviation from normal operating voltage to 49% of nominal. The inverter should disconnect in 6 cycles or less.
Test 2. A deviation from normal operating voltage to 87% of nominal. The inverter should disconnect in 120 cycles or less.
Test 3. A deviation from normal operating voltage to 111% of nominal. The inverter should disconnect in 120 cycles or less
Test 4. A deviation in voltage from nominal to 138% of nominal. The inverter should disconnect in 2 cycles or less.

3.2.4.3 Frequency disturbances

The conditions of concern are from paragraph 5.1.2 of IEEE P929. Annex G further defines the frequency slew rate to be no faster than 0.5 Hz/s. Local loads are not specified for this test. The inverter should provide no energy to the utility within 6 cycles after experiencing the following two conditions.

Test 1. Frequency will be ramped from 60 Hz to 60.6 Hz with a slew rate < 0.5 Hz/s then maintained at 60.6 Hz.. Disconnect time will be measured from the time the frequency is greater than 60.5 Hz.

Test 2. Frequency will be ramped from 60 Hz to 59.2 Hz with a slew rate < 0.5 Hz/s then maintained at 59.2 Hz. Disconnect time will be measured from the time the frequency is less than 59.3 Hz.

3.2.5 Loss of utility with special load conditions (anti-islanding)

These tests will be performed using the DETL grid. For an inverter to pass these tests it must incorporate active "non-islanding means" thereby satisfying the requirements of the new distributed generation interconnection standard IEEE 1547 (Section 5.5.1 "Unintentional Islanding").[3] The utility will be disconnected under two types of load conditions as specified in IEEE 929 and UL 1741 tests for a "non-islanding inverter." The two types of loads are: 1) matched, resonant RLC and 2) mismatched power or power factor. The matched, resonant RLC load has been determined to be the local load condition under which loss of utility is most difficult to detect. A simplified one-line diagram of the test setup is shown in figure 1. For each anti-islanding test, the grid is removed with a given set of local load conditions, and the time required for the inverter to cease to energize its output is recorded. If any of these tests results in islanding for longer than the time specified, the unit fails the test and the test sequence is considered complete.

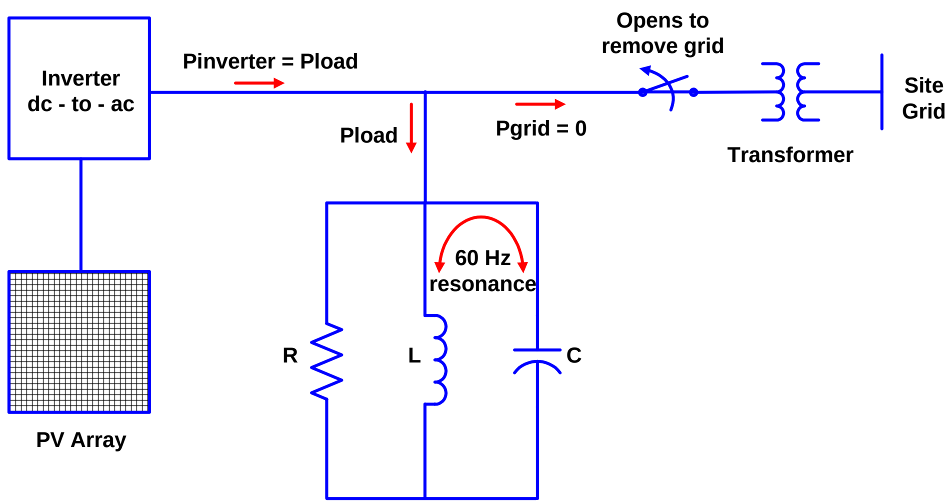

Figure 1. Islanding Test One-Line Diagram

3.2.5.1 Matched Resonant RLC Load (44 tests)

This test represents a low-probability load condition under which loss of utility is extremely difficult to detect. IEEE 929 and UL 1741 require that the generation source shut down within two seconds following loss of utility with this load. Tests will be performed at 25%, 50%, 75%, and 100% of rated power. At each power level, the resistive load will be adjusted to absorb all real power from the inverter, and the inductive and capacitive loads will be adjusted to absorb all reactive power from the inverter. The RLC tank circuit will be adjusted to have a quality factor (vars/Watts ratio) of 2.5 and will then be tuned for 60-Hz resonance.

Following a test at a given power level, either L or C will be adjusted by ±1% (to a maximum of ±5%). The test will be repeated so that a total of eleven tests are performed at each power level. The maximum disconnect time will be reported.

3.2.5.2 Matched Resistive Load (1 test)

The inductive and capacitive elements will be removed from the circuit and the test repeated with a resistive load adjusted to match the power output of the inverter. This test will be performed at

[3] IEEE 1547-2003, Standard for Interconnecting Distributed Resources With Electric Power Systems

close to rated power. For this special case that is not specifically addressed in IEEE 929, the inverter should cease to energize its output within two seconds following loss of utility.

3.2.5.3 Mismatched Loads (20 tests)

For these anti-islanding tests, either the real or the reactive power to the load will be mismatched to the inverter output. There is a much higher probability that there will be at least this degree of mismatch between generation and local load at any given time. To minimize possible interference with high-speed recloser operations, IEEE 929 and UL 1741 require that the inverter cease to energize its output within ten cycles following loss of utility with these loads. Each of the following tests will be repeated five times.

Test 1. resistive load with a P_{gen}/P_{load} ratio of 1.5
Test 2. resistive load with a P_{gen}/P_{load} ratio of 0.5
Test 3. RC load with a power factor of .94 leading
Test 4. RL load with a power factor of .94 lagging

3.2.5.4 Multiple Inverters on a Common AC Line

There are additional complexities when multiple inverters are running in parallel. Two “non-islanding” inverters of different types will be operated on the same branch circuit with a local load. A resistive load will be matched to the inverters’ combined output power. Utility power will be interrupted and the disconnect time for each inverter will be measured. Power will be reconnected after 30 seconds and the restart of each inverter will be monitored. IEEE 929 or UL 1741 does not require this test.

3.3 Electromagnetic Interference

Radio-frequency interference (rfi) will be measured and compared to FCC limits. In FCC Part 15B, Class A limits pertain to commercial and industrial facilities, and Class B to residences. Measurements will be taken with a Farnell SSA 1000A spectrum analyzer. Because dc power supplies may generate rfi, these tests are performed using solar input power. The procedures for RFI tests at DETL are detailed separately.

3.3.1 Conducted RFI (450 kHz – 30 MHz)

Conducted EMI will be measured on both the ac and dc lines. The conducted signal may be measured in either of two manners.[4] The first uses a LISN (line stabilization network) whose purpose is to provide uniform impedance between the device under test and the line. The LISN provides a monitoring point. This approach should provide consistent measurements when conducted in different locations; however, the conducted emissions in the final situation are likely to differ somewhat from those measured.

The second approach utilizes a line probe. This approach is easier to implement and provides exactly the correct answer when the test is conducted in situ. When used in a laboratory environment, the line probe answer will provide a slightly different result from those in measured in the installed system.

3.3.2 Radiated RFI (30 MHz – 1 GHz)

Measurements will be made using a Farnall RFI antenna designed for the purpose and placed at a distance of 3 meters from the inverter. Closer measurements will result in higher magnitude

[4] FCC/OET MP-4 (1987), FCC Procedure for measuring rf Emissions from Computing Devices

signals. The approach used at Sandia for these measurements is to record the radiated rfi and ignore the narrow band spikes from local radio stations. Rfi energy generated from switching devices is wide-band, and thus will fill the space between narrow-band signals. It is easily detected as a rise in the noise floor. Oscillators and clocks in inverters are so far below 30 MHz that they do not contribute to the radiated signals. An SNL test procedure details the test methodology.

3.4 Surge Protection

Provide all inverter inputs with the following pulses[5&6&7].,

- 100 kHz ring wave (6 kV open circuit)
- 1.2 by 50 microsecond (6 kV open circuit)
- 8 by 20 microsecond (3 kA short circuit) pulse

Pulse levels will initiate at 1,000 volts (open circuit voltage) and increment up to 6,000 volts in 1,000-volt steps. Measure pulse levels which are coupled through surge protection circuits. Because of the potential for inverter damage, this will be the last test. The transfer functions are provided to the manufacturer. Any effect of pulsing and the voltage level where the effect is noted will be recorded.

3.5 User Issues

User issues include reliability and usability. A reliable system has minimal unscheduled downtime, including failures and nuisance trips. A useable system causes the customer few problems. Operational transparency of the entire system to the homeowner has been identified as a key marketing feature for residential PV systems.

3.5.1 Acoustic Noise

Measurements will be made using the calibrated B&K microphone with the A filter selected. Measurements will be taken when background noise is negligible; preferably less than 50 dB. The microphone will be placed on a tripod at a distance of 0.5 meters from the inverter, and a single noise reading in dB will be recorded. Spectral information, which may be valuable for identifying the source of the noise, will be recorded with the C filter in use. These measurements are for general information only. Acoustic measurements requiring high precision and reproducibility, for example, those that are to be used for compliance certification, should be made using either an anechoic chamber or a system capable of calculating sound power.

3.5.2 Nuisance Trips

Any unplanned trips or reconnection times longer than the IEEE 929 recommendation (currently 5 minutes) will be recorded.

3.5.3 Features

Presence of any of the following features will be documented.

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[5] ANSI C37.90.1-1989, Standard Surge Withstand Capability (SwC) Tests for Protective Relays and Relay Systems

[6] IEEE C62.41-1991, Recommended Practice on Surge Voltages in Low-Voltage AC Power Circuits

[7] UL 1741, Static Inverters and Charge Controllers for use in Photovoltaic Power Systems, 1st Edition, May 7, 1999

feature	**Yes**	**No**	**Comments**
diagnostic receptacle			
on/off switch			
maintenance disconnects			
diagnostics			
indicators			
ground fault detection			
smoke detector			
over temperature shutdown			
mode indicator			
over current protection[8]			
grounding lugs			
markings[9]			
remote disable			
remote restart			
surge arrestors (ac)			
surge arrestors (dc)			
other			

[8] National Electrical Code Article 690-9
[9] National Electrical Code Article 690-52